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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
FERRIS III, FRED O	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/737,347	STUECHELI, JEFFREY ADAM	
	Examiner	Art Unit	
	Fred Ferris	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,10-14 and 19* is/are rejected.

7)☒ Claim(s) *6-9,15-18 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *04112005*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

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DETAILED ACTION

1. This Office Action is in response to applicant's request for reconsideration filed 11 March 2005. Claims 1-5, 10-14, and 19 remain rejected by the examiner. Claims 6-9, 15-18 and 20 are objected to.

Response to Arguments

2. Applicant's arguments filed on 11 March 2005 requesting reconsideration have been fully considered but are not persuasive.

During applicants telephone interview of 10 March 2005 the examiner agreed to reconsider the rejection of claims 1-5, 10-14, and 19 in view of applicant's arguments, and any amendments to the claims. Upon review of the prior art, and in consideration of applicant's arguments filed 11 March 2005, the examiner believes that the claimed limitations are obvious in view of the prior art for the following reasons:

Regarding applicant's response to 103(a) rejection: Applicants arguments have focused on the prior art (Aharon and Dey) as not teaching "generating a driver model having a plurality of states, wherein each state indicates whether to drive an interface of the hardware model", as recited in independent claims 1, 10, and 19. The examiner maintains that this limitation is obvious in view of the prior art. Specifically, that a skilled artisan having access to the teachings of Aharon and Dey would have had sufficient technical direction and motivation to realize a driver model having multiple states which indicate whether to drive a hardware interface within the context of the subject matter as claimed by applicants. The examiner's reasoning is as follows.

First, the examiner notes that this limitation is extremely broad in scope and breadth. For example, the process of "generating a driver model having a plurality of states" can simply be interpreted as generating (or creating by any means) a driver (i.e. computer code) having multiple states that indicates whether to drive (or not drive) a hardware interface (again, of any type). The recited "model" for the hardware and driver can simply be interpreted to be any mathematical or graphical representation of a real world situation or object (Microsoft Computer Dictionary, 3rd Edition) As cited in the office action, the drivers disclosed by Aharon have "states" that indicate how, or how not to, "drive" the hardware based on a set of conditions that determine the driver's current state. (CL2-46-49) That is, Aharon discloses how a skilled artisan would "model" a driver for a hardware interface. The examiner has therefore interpreted applicant's driver model process to be functionally equivalent to the driver control process disclosed by Aharon.

MPEP 2106 recites the following supporting rational:

> "While it is appropriate to use the specification to determine what applicant intends a term to mean, a positive limitation from the specification cannot be read into a claim that does not impose that limitation. A broad interpretation of a claim by Office personnel will reduce the possibility that the claim, when issued, will be interpreted more broadly than is justified or intended. An applicant can always amend a claim during prosecution to better reflect the intended scope of the claim."

Second, looking into applicant's specification for guidance on the specific meaning of the term "driver model" does not provide a clear distinction of the limitation over the prior art and is, in fact, somewhat ambiguous. For example, the passages on page 10, lines 21-23 of the specification indicate that the Markov model used to describe whether to drive the interface, is referred to as the "driver model". This

definition appears to be rendered ambiguous by the passages on page 9, line 16 of applicant's specification which states that the driver module (not driver model) actually creates a subgraph of Markov models. These passages appear offer multiple interpretations of the claimed subject matter. For example, is the claimed "driver model" actually the driver module, or is the "driver model" simply a well-known Markov chain? As noted on pages 13-14 of the office action, a Markov chain is merely "a random process where the probability that certain state will occur depends only on the present or preceding state of the system, and not the events leading up to the present state". (Encyclopedia of Computer Science, Mason/Charter, 1976) Markov chains are well known to those skilled in the art and are commonly used as a method of generating random samples from a probability space and, hence, would have been an obvious choice to one skilled in the art.

Applicants have also argued that Figure 4, and the passages recited on specification page 9-10 referring to the "a probability of .01 or 1%" and "a probability of .99 or 99%" of returning/transitioning to a state, distinguish the claimed inventions "plurality of states for a driver model" over the prior art. However, it is noted that these features are not recited in the language of the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See In re Van Geuns, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Applicants have also argued that the prior art Dey does not teach or suggest generating a driver model having a plurality of states and that prior art Asher does not teach or mention drivers. In response to applicant's arguments against these references

individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See In re Keller, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Further, the test for obviousness is what the combined teachings of the references would have suggested to one of ordinary skill in the art (see: MPEP 2143.01). The examiner therefore assets that the claimed limitations relating to "generating a driver model having a plurality of states, wherein each state indicates whether to drive an interface of the hardware model" are rendered obvious in view of the prior art.

Regarding applicant's comments on motivation to combine: The examiner disagrees with applicants position the examiner's motivation to combine is improper and has not merely stated that the modification "would be obvious to one skilled in the art", as alleged by applicants. The examiner maintains that the motivation to combine Aharon and Dey is proper and in accordance with MPEP guidelines for the following reasons. MPEP 2143.01 Suggestion or Motivation To Modify the References first recites:

"There are three possible sources for a motivation to combine references: the nature of the problem to be solved, the teachings of the prior art, and the knowledge of persons of ordinary skill in the art." In re Rouffet, 149 F.3d 1350, 1357, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998)

In this case the examiners rejection first addresses the nature of the problem to be solved, namely, generating pseudo random test patterns against a hardware model and using a random walk technique, relative to the teachings in the prior art. (Office Action page 7, line 3) The examiner first references the prior art (Aharon, CL7-L49-67)

which discloses that random selection of test patterns is important in generating a sequence of test patterns because of the high probability selecting the same pattern (instruction) during the generation of a test pattern sequence. The examiner also cited other prior art such as David, Carletta, Bauman , and Gluska (office action page 13) as teaching test pattern generation. Here, the examiner has established that the market is competitive (crowded), with many known methods and systems for generating random test patterns in the market place as would be easily recognized by a person skilled in the art. Therefore, in suggesting a motivation to combine, the examiner specifically focused his motivation on the knowledge of persons of ordinary skill in the art. More specifically, that a skilled artisan would have made an effort to become aware of what capabilities had been developed in the market place, and hence would have knowingly modified Aharon with the teachings of Dey. MPEP 2144 Sources of Rationale Supporting a Rejection Under 35 U.S.C. 103 recites:

> "The rationale to modify or combine the prior art does not have to be expressly stated in the prior art; the rationale may be expressly or impliedly contained in the prior art or it may be reasoned from knowledge generally available to one of ordinary skill in the art, established scientific principles, or legal precedent established by prior case law. In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). See also In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) (setting forth test for implicit teachings); In re Eli Lilly & Co., 902 F.2d 943, 14 USPQ2d 1741 (Fed. Cir. 1990) (discussion of reliance on legal precedent); In re Nilssen, 851 F.2d 1401, 1403, 7 USPQ2d 1500, 1502 (Fed. Cir. 1988) (references do not have to explicitly suggest combining teachings)"

In this case, the examiner has simply asserted that a skilled artisan tasked with solving the problem of generating pseudo random test patterns (i.e. as taught by Aharon), and knowing that the randomness of the selection of test patterns is important (Dey teaches improved randomness using a "random walk"), and further having access to the teachings of Aharon and Dey, would have knowingly modified the teachings of

Aharon, with the teachings of Dey in order to gain the advantage of an improved randomness in the generation of test patterns. (There is also an additional benefit of reducing the development time and cost) Specifically, a skilled artisan working in this obviously competitive environment would have made an effort to become aware of what capabilities had already been developed in the market place, and hence would have been aware of, and known to seek out the relative teachings of the problem to be solved. Namely, the teachings of Aharon and Dey.

MPEP 2143.01 Suggestion or Motivation To Modify the References further recites the following supporting rational:

> Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. **"The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art."** In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000).

The examiner therefore appears to have established an implicit showing that in view of the combined teachings of the prior art, the relative knowledge of one skilled in the art, and in particular, the nature of the problem to be solved, there exists an obvious motivation to combine the references as noted above.

Accordingly, the examiner maintains the 103(a) rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 2, 10, 11, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,202,889 issued to Aharon et al in view of "Exploiting Hardware Sharing in High-Level Synthesis for Partial Scan Optimization", S. Dey et al, IEEE 1063-6757/93, IEEE 1993.

Independent claim 1 is drawn to:

method for generating pseudo random test patterns simulating hardware model by:
- generating driver model having states where each state indicates whether to drive an interface of hardware model;
- initiating random walk through driver model to generate driver test pattern;
- controlling simulation of hardware model using driver test pattern.

Regarding independent claim 1: Aharon discloses a method and system for generating pseudo random test patterns (CL1-L21-31) for producing simulated test scenarios against a hardware model (CL1-L51-61). Aharon discloses the elements of the claimed limitations of the present invention as follows:

- generating driver model having states where each state indicates whether to drive an interface of hardware model: Aharon discloses test programs (patterns) that are simulated against a hardware model under driver control (CL2-L46) where the drivers can change the conditions with which the test programs are executed (CL2-L49). That is, the drivers disclosed by Aharon have "states" that indicate how, or how not to, "drive" the hardware model based on a set of conditions that determine the driver's current state. The examiner interprets applicant's driver model process to be functionally equivalent to the driver control process disclosed by Aharon.

- controlling simulation of hardware model using driver test pattern: Aharon discloses generating pseudo random test patterns (CL1-L21-31) under driver control (CL2-L47) of a simulated design model (CL1-L60). That is, the test patterns are simulated against a hardware design model (CL2-L46), while the drivers controlling the test patterns (CL2-L48) can change the test conditions under which the test patterns are executed (CL2-L48), based on the current state of the driver (CL2-L47).

Aharon does not explicitly disclose using a random walk through the model to generate the driver test pattern.

- initiating random walk through driver model to generate driver test pattern: Dey teaches using a random walk technique (page 23, col. 2, para: 4, Section 4.1) in the modeling of scan variables (test vectors) used for gate level hardware testing. The examiner notes that techniques such as random walks, table walks, walking

bits, etc. are generally well-known to those skilled in the art and, hence, would have been an obvious choice for implementing the walk through the drive model, in addition to being taught by Dey. (See: Dey, Section 4.1)

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to modify the teachings of Aharon relating to generating pseudo random test patterns against a hardware model, with the teachings of Dey relating to using a random walk technique on the driver model, to realize the claimed invention. An obvious motivation exists since, as referenced in the prior art, random selection of test patterns (instructions) is important in generating a sequence of test patterns because of the high probability selecting the same pattern (instruction) during the generation of a test pattern sequence (See Aharon, CL7-L49-67). Accordingly, a skilled artisan having access to the teachings of Aharon and Dey would have knowingly modified the teachings of Aharon with the teachings of Dey, in order to improve the randomness of the generation of the driver test patterns, and provide a more exhaustive test pattern sequence.

Per dependent claim 2 - each state comprises drive state and wait state: Aharon discloses controlling test patterns by driver state as noted above (CL2-L46-49). Aharon further discloses the use of "loop" logic in "waiting" to obtain the desired sequences for test patterns. (i.e. an equivalent function to wait states) The examiner notes that the use of "wait states" is very well known in the art as a way of having a process "wait" for data results (See: "wait state", Microsoft Dictionary, Third Edition, 1997).

Independent claim 10 is drawn to:

Apparatus for generating pseudo random test patterns simulating hardware model by:
- generating driver model having states where each state indicates whether to drive an interface of hardware model;
- initiating random walk through driver model to generate driver test pattern;
- controlling simulation of hardware model using driver test pattern.

Regarding independent claim 10: As previously cited above, Aharon discloses a method and system (apparatus) for generating pseudo random test patterns (CL1-L21-31) for producing simulated test scenarios against a hardware model (CL1-L51-61). Aharon discloses the elements of the claimed limitations of the present invention as follows:

- means for generating driver model having states where each state indicates whether to drive an interface of hardware model: Aharon discloses test programs (patterns) that are simulated against a hardware model under driver control (CL2-L46) where the drivers can change the conditions with which the test programs are executed (CL2-L49). That is, the drivers disclosed by Aharon have "states" that indicate how, or how not to, "drive" the hardware model based on a set of conditions that determine the driver's current state. Aharon therefore discloses the "means for" generating a driver model interfacing (controlling) a hardware model. The examiner interprets applicant's driver model process to be functionally equivalent to the driver control process disclosed by Aharon.

- means for controlling simulation of hardware model using driver test pattern: Aharon discloses generating pseudo random test patterns (CL1-L21-31) under

driver control (CL2-L47) of a simulated design model (CL1-L60). That is, the test patterns are simulated against a hardware design model (CL2-L46), while the drivers controlling the test patterns (CL2-L48) can change the test conditions under which the test patterns are executed (CL2-L48), based on the current state of the driver (CL2-L47). Aharon therefore discloses the "means for" controlling hardware model simulation using a driver test pattern.

Aharon does not explicitly disclose using a random walk through the model to generate the driver test pattern.

- means for initiating random walk through driver model to generate driver test pattern: Dey teaches using a random walk technique (page 23, col. 2, para: 4, Section 4.1) in the modeling of scan variables (test vectors) used for gate level hardware testing. Dey therefore discloses the "means for" initiating a random walk. The examiner notes that techniques such as random walks, table walks, walking bits, etc. are generally well-known to those skilled in the art and, hence, would have been an obvious choice for implementing the walk through the drive model, in addition to being taught by Dey. (See: Dey, Section 4.1)

It would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to modify the teachings of Aharon relating to generating pseudo random test patterns against a hardware model, with the teachings of Dey relating to using a random walk technique on the driver model, to realize the claimed invention. An obvious motivation exists since, as referenced in the prior art, random

selection of test patterns (instructions) is important in generating a sequence of test patterns because of the high probability selecting the same pattern (instruction) during the generation of a test pattern sequence (See Aharon, CL7-L49-67). Accordingly, a skilled artisan having access to the teachings of Aharon and Dey would have knowingly modified the teachings of Aharon with the teachings of Dey, in order to improve the randomness of the generation of the driver test patterns, and provide a more exhaustive test pattern sequence.

Per dependent claim 11 - each state comprises drive state and wait state: Aharon discloses controlling test patterns by driver state as noted above (CL2-L46-49). Aharon further discloses the use of "loop" logic in "waiting" to obtain the desired sequences for test patterns. (i.e. an equivalent function to wait states) The examiner notes that the use of "wait states" is very well known in the art as a way of having a process "wait" for data results (See: "wait state", Microsoft Dictionary, Third Edition, 1997).

Regarding independent claim 19: Independent claim 19 merely claims the computer program code for the same limitations as recited in independent claims 1 and 11 and is therefore rejected using the same reasoning as previously cited above.

4. Claims 3 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,202,889 issued to Aharon et al, in view of "Exploiting Hardware Sharing in High-Level Synthesis for Partial Scan Optimization", S. Dey et al, IEEE

1063-6757/93, IEEE 1993, in further view of U.S. Patent 6,163,876 issued to Asher et al

As recited above, the combination of Aharon and Dey renders obvious the elements of the claimed limitations of independent claims 1 and 10. (see rejection of claims 1 and 10 above) However, the combination of Aharon and Dey further does not explicitly teach the use of a sub-graph connecting the driver model as recited in dependent claims 3 and 12.

Per dependent claims 3 and 12 – (means for) creating driver sub-graph having states & connecting sub-graph to form driver model: Ashar teaches the use of sub-graphs having multiple states (CL9-L30, L61-65, CL10-L4, Fig 1b) in the verification and testing of a hardware model (CL5-L11, CL10-L12-17) and connecting the sub-graphs (Fig. 1b) according to state. The examiner notes that, in addition to being disclosed by Asher, sub-graphs are merely a subset of the nodes and edges of a well-known graph data structure (See: "graph (subgraph)", Microsoft Dictionary, Third Edition, 1997) and, hence, would have been an obvious choice to one skilled in the art for connecting the driver model at the time of the invention. Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to further modify the combined teachings of Aharon and Dey as previously noted above, with the teaching of Asher relating to connecting the sub-graphs in forming the driver model, in order to improve the randomness of the generation of the driver test patterns, and provide a more exhaustive pattern sequence.

5. Claims 4, 5, 13 an 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,202,889 issued to Aharon et al, in view of "Exploiting Hardware Sharing in High-Level Synthesis for Partial Scan Optimization", S. Dey et al, IEEE 1063-6757/93, IEEE 1993, in further view of U.S. Patent 6,163,876 issued to Asher et al, and in further view of U.S. Patent 5,500,941 issued to Gil.

As recited above, the combination of Aharon, Dey, and Asher renders obvious the elements of the claimed limitations of independent claims 1 and 10 and dependent claims 3 and 12. (see rejection of claims 1, 10, 3, and 12 above) However, the combination of Aharon, Dey, and Asher further does not explicitly teach the use of a Markov chain or probability of transitioning between states as recited in dependent claims 4, 13 and 5, 14 respectively.

Per dependent claims 5 and 14 - probability of state transitioning: Gil discloses calculating the probabilities of the occurrence of state transitions from one state to another (CL4-L55, CL6-L38-40, Fig 4).

Per dependent claims 4 and 13 - Markov chain: Gil discloses the use Markov chains for generating state transition using during testing. (CL4-L47-56, Fig. 1)

The examiner again notes that, in addition to being disclosed by Gil, a Markov chain is merely "a random process where the probability that certain state will occur depends only on the present or preceding state of the system, and not the events leading up to the present state". (Encyclopedia of Computer Science, Mason/Charter, 1976) Markov chains are well known to those skilled in the art and are commonly used

as a method of generating random samples from a probability space and, hence, would have been an obvious choice to one skilled in the art for implementing in the driver sub-graph. Therefore, it would have been obvious to one of ordinary skill in the art at the time the claimed invention was made to further modify the combined teachings of Aharon, Dey, Asher, as previously noted above, with the teaching of Gil relating to Markov chain probability, in order to improve the randomness of the generation of the driver test patterns, and provide a more exhaustive pattern sequence.

Allowable Subject Matter

6. Claims 6-9, 15-18 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In particular, the prior art of record does not specifically disclose the command model to generate the command test pattern as recited claims 6-9, 15-18 and 20. Applicant's specification has defined the term "command model" as the model used to describe the commands to send across the interface and operates as disclosed in the passages on page 10, line 21 to page 12, line 17 of the specification.

Conclusion

7. ***THIS ACTION IS MADE FINAL.*** *Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).*

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Careful consideration should be given prior to applicant's response to this Office Action.

U.S. Patent 6,381,715 issued to Bauman et al teaches test pattern generation for hardware models.

U.S. Patent 5,592,674 issued to Gluska et al teaches test pattern generation and Markov chains.

"Random Pattern Testing Versus Deterministic Testing of RAM's", R. David et al, IEEE Transactions on Computer, Vol. 38, No. 5, May 1989 teaches test pattern generation.

"A Method for Testability Analysis and BIST Insertion at the RTL", J. Carletta et al, IEEE 1066-1409/95, IEEE 1995 teaches test pattern generation.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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